PATENT ABSTRACTS OF JAPAN

(11)Publication number : **09-009251**
(43)Date of publication of application : **10.01.1997**

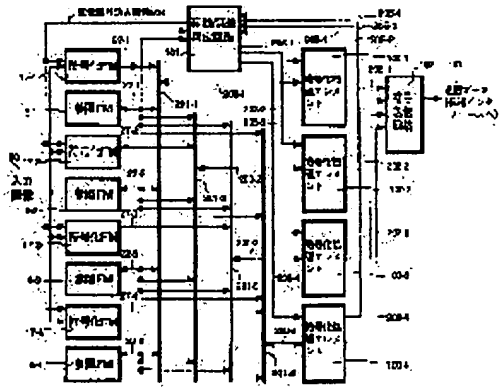
(51)Int.Cl. **H04N 7/24**

(21)Application number : **07-152860**
(22)Date of filing : **20.06.1995**

(71)Applicant : **HITACHI LTD**
(72)Inventor : **SHIMURA TAKANORI**
KATO JUNICHI

(54) PARALLEL PICTURE ENCODING METHOD AND DEVICE THEREFOR

(57)Abstract:
PURPOSE: To reduce power consumption in the case of encoding dynamic images.
CONSTITUTION: An image encoding device for encoding the dynamic images is provide with a valid/invalid judgement circuit 101 for storing the result of judging whether respective image blocks in one screen are valid or invalid and plural encoding processing elements 100-i for performing an encoding processing corresponding to the number of the valid blocks within one screen calculated in the valid/invalid judgement circuit 101. Then, the required encoding processing element 100-i is selected and activated from the plural encoding processing elements corresponding to the ratio of the valid blocks for which a processing amount is large.



(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号

特開平9－9251

(43)公開日　平成９年(1997)１月10日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０４Ｎ　7/24			Ｈ０４Ｎ　7/13	Ｚ

審査請求　未請求　請求項の数８　ＯＬ　（全９頁）

(21)出願番号　特願平7－152860

(22)出願日　平成７年(1995)６月20日

(71)出願人　000005108
株式会社日立製作所
東京都千代田区神田駿河台四丁目６番地

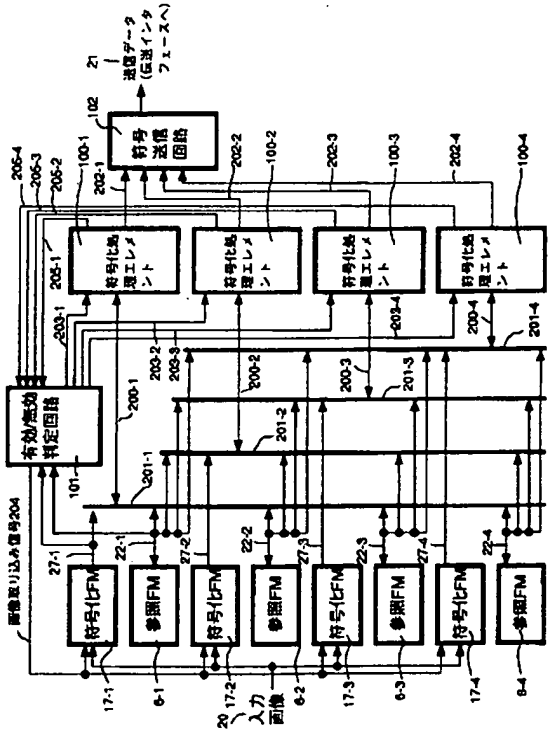
(72)発明者　志村　隆則
東京都国分寺市東恋ケ窪１丁目280番地
株式会社日立製作所中央研究所内

(72)発明者　加藤　淳一
東京都国分寺市東恋ケ窪１丁目280番地
株式会社日立製作所中央研究所内

(74)代理人　弁理士　磯村　雅俊

(54)【発明の名称】　並列画像符号化方法およびその装置

(57)【要約】
【目的】動画像を符号化する場合に、低消費電力化を実現する。また、携帯型の情報通信端末を開発する場合に、画像符号化装置を提供する。
【構成】動画像を符号化する画像符号化装置において、１画面の中の各画像ブロックが有効か無効かの判定結果を格納する有効／無効判定回路と、有効／無効判定回路で算出した１画面内の有効ブロック数に応じて符号化処理を行う複数の符号化処理エレメントとを具備し、処理量が多い有効ブロックの割合に応じて複数の符号化処理エレメントの中から必要な符号化処理エレメントを選択して起動させる。



1

【特許請求の範囲】

【請求項１】一つ前に符号化復号化された参照画像を格納しておく参照画像記憶手段と、
該参照画像と次に符号化する現画像とを特定の画素単位ブロック毎に差分をとり、該差分の大きさに応じて該画素単位ブロック毎に動きのない無効ブロックに対する無効処理と、動きのある有効ブロックに対する有効処理とに符号化方法を変える有効／無効判定手段と、
該有効／無効判定手段からの起動信号により現画像を分割し、それぞれが並列に符号化復号化する複数の符号化処理手段と、
該複数の画像符号化処理手段からの出力である符号化されたデータの伝送順序を制御する符号送信手段とを有することを特徴とする並列画像符号化装置。

【請求項２】参照画像と現画像の二つの画像から該現画像の符号化を行うとともに、次の画像の符号化に必要な参照画像を作成する動画像の符号化方法において、
１画面内の有効ブロックの数を算出し、
整全体のブロックに対する該有効ブロックの比率が高い場合には、符号化処理の並列度を高め、
該有効ブロックの比率が小さい場合には、符号化処理の並列度を下げるようにしたことを特徴とする並列画像符号化方法。

【請求項３】請求項１に記載の画像符号化装置において、前記有効／無効判定手段と符号化処理手段と符号送信手段とを集積回路で構成したことを特徴とする並列画像符号化装置。

【請求項４】請求項２に記載の画像符号化方法において、前記符号化処理の並列度を高めたり、低下させたりするとともに、
現画像を分割して並列に符号化する場合に、各符号化処理手段に割り当てられた有効ブロックの比率が同じ数に近づくように現画像を複数に分割し、
それぞれ分割した画像を各符号化処理手段に分配し、
各符号化処理手段で並列に符号化することを特徴とする並列画像符号化方法。

【請求項５】一つ前に符号化復号化された参照画像を格納しておく参照データ記憶手段と、
該参照画像と次に符号化する現画像とを特定の画素単位ブロック毎に差分をとり、該差分の大きさに応じて該画素単位ブロック毎に動きのない無効ブロックに対する無効処理と、動きのある有効ブロックに対する有効処理とに符号化方法を変える有効／無効判定手段と、
該有効／無効判定手段からの有効ブロック数情報に応じて動作クロックを制御するクロック制御手段と、
該クロック制御手段からのクロックにより動作する画像符号化処理手段とを有することを特徴とする画像符号化装置。

【請求項６】参照画像と現画像の二つの画像から該現画像の符号化を行うとともに、次の画像の符号化に必要な

2

参照画像を作成する動画像の符号化方法において、
１画面内の有効ブロックの数を算出し、
有効ブロックの比率が高い場合には、符号化処理回路のクロック周波数を高くし、
有効ブロックの比率が小さい場合には、該符号化処理回路のクロック周波数を下げることを特徴とする画像符号化方法。

【請求項７】請求項１に記載の並列画像符号化装置において、前記符号化処理手段をマイクロコンピュータで構成することを特徴とする並列画像符号化装置。

【請求項８】請求項１に記載の並列画像符号化装置において、前記符号化処理手段をディジタルシグナルプロセッサで構成することを特徴とする並列画像符号化装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、ディジタル回線および無線回線を利用して圧縮した画像を伝送するテレビ（以下TV）電話やTV会議などの画像符号化方法において、消費電力の少ない並列画像符号化方法およびその装置に関するものである。

【０００２】

【従来の技術】従来より画像符号化方法としては、一般的に駒落し法が広く知られている。通常のTV信号（NTSC信号）が毎秒３０フレーム（６０フィールド）で２駒を送信側から伝送しているのに対して、駒落し法では、例えば二つのフィールド内の片方のみを伝送して毎秒３０駒で伝送したり、上記片フィールドをさらに間引いて毎秒１５駒以下で伝送する方法である。受信側では、伝送された同一の駒を複数回表示することにより、伝送すべき信号量の削減を可能にしている。例えば、TV放送では１秒間に３０枚～６０枚で送っており、人間の目には駒落しとは感じられないが、電話回線等のように伝送路の容量に制限されて、１秒間に１０枚～１５枚しか送れない場合には、人間の目には違和感を覚える。しかし、TV会議やTV電話等のように被写体の動き量が比較的小さい場合には、駒落し法を実施しても違和感の小さいことが実験的に知られている。これに加えて「離散コサイン変換等の直交変換」，「量子化」，「フレーム間予測」，「動き補償フレーム間予測」等の信号処理により、画像信号を高能率符号化して伝送することが可能になってきている。この中で単純フレーム間予測，および動き補償フレーム間予測は、直前に符号化されたフレーム信号を参照して次のフレームを予測符号化する方法である。これらの符号化方式と直交変換を組み合わせると、大幅な冗長度圧縮が可能となることから、ITU-T（旧CCITT：国際電信電話諮問委員会）で勧告されている動画像符号化方式（H.261）でも採用されている。

【０００３】上述の動画像符号化方式の画像符号化装置を実現する場合、伝送路の伝送速度が大きく影響する。伝送路が高速である場合（例えば、転送速度1.5Mbps）

には、伝送できる情報量が多いため、品質の良い（動きの速い）画像を符号化復号化できることが期待できるが、その反面、1秒間に30フレームの高速処理を実現できる高価なハードウエアを開発することが必要とされる。一方、伝送路が低速である場合（例えば、転送速度64kbps）には、伝送できる情報量が少ないため、画質は劣化（動きが遅い駒落し画像、1秒間に5～15フレーム）するものの、低価格なハードウエアで実現することが可能となる。そこで、伝送速度に応じて別々のハードウェアを開発した場合には、当然のことながら開発コストがかかってしまう。結局、伝送速度が低速な場合に動作するハードウェアを一つ開発しておき、これを複数個配置して並列処理させるようにして、伝送速度が高速な場合でも適用できる並列処理可能なハードウェアを実現することにより、開発コストを大幅に削減することが可能となる。

【0004】

【発明が解決しようとする課題】従来の並列処理を実現する画像符号化装置としては、例えば特開平5－3046633号公報に記載された「画像符号化装置」がある。それまでは並列処理方式においても画質を改善することに重点が置かれていた。しかしながら、画像符号化装置を並列化するときには、演算処理装置の並列化による消費電力の増加が問題となる。特に携帯型装置の場合には、電池やバッテリで動作させる必要があるため、消費電力に関しての改善が不可欠である。本発明の目的は、このような従来の課題を解決し、携帯型の情報端末で画像を伝送して画像を符号化復号化する場合に、できるだけ電力消費の少ない並列画像符号化方法およびその装置を提供することにある。

【0005】

【課題を解決するための手段】上記目的を達成すめため、本発明の並列画像符号化方法では、①一つ前に符号化復号化された画像データ（参照画像）と、次に符号化する画像データ（現画像）とを特定の画素単位であるブロック（例えば8画素×8ライン）毎に相関をとり、相関が小さいときは動きのない無効ブロックとみなし、一方、相関が大きいときは動きのある有効ブロックとみなし、1画面内の有効ブロックの数を算出して、処理量の多い有効ブロック数が多い場合には1画面を複数の領域に分割し、分割した領域毎に符号化処理を行う符号化処理回路を動作させ、また有効ブロック数が少ない場合には1画面の分割を少なくし（または、分割しなくてもよい）、分割した領域毎に動作させる符号化処理回路の数を少なくすることにより、低消費電力化を図る。また、②参照画像と現画像とを特定のブロック毎に相関をとり、相関が小さいときには動きのない無効ブロックとみなすが、相関が大きいときは動きのある有効ブロックとみなし、1画面内の有効ブロックの数を算出し、有効ブロック数に応じて1画面の画像を分割して並列に符号化

する場合に、分割した領域内での有効ブロックの比率が同じ数に近づくように1画面の画像を分割し、それぞれ分割した画像を並列に符号化するようにして、低消費電力化を図る。

【0006】また、本発明の並列画像符号化方法では、③参照画像と現画像とをブロック毎に相関をとり、相関が小さいときには動きのない無効ブロックとみなし、相関が大きいときには動きのある有効ブロックとみなして、1画面内の有効ブロックの数を算出し、有効ブロックの比率が高い場合には、符号化処理を行う符号化処理回路のクロック周波数を高くし、少ない場合には、符号化処理回路のクロック周波数を下げるようにすることで、低消費電力化を図る。また、④このように並列に配置して動作させる符号化処理回路を、低消費電力のマイクロコンピュータで実現することにより、低消費電力化を図る。また、⑤このように並列に配置して動作させる符号化処理回路を、動作速度の速いディジタルシグナルプロセッサで実現する。さらに、⑥有効／無効を判定する有効／無効判定回路と、並列に符号化を行う複数個の符号化処理回路と、これらの符号化処理回路で符号化されたデータを選択して伝送する符号送信回路をそれぞれLSIのマクロブロックとして設計することにより、これを1チップ化する。

【0007】

【作用】本発明においては、情報通信端末装置に実装する画像符号化装置で画像の符号化・復号化を行う場合、処理量が多い有効ブロックの割合に応じて複数の符号化処理回路の中から処理量に必要な符号化処理回路を選択して、これを起動し動作させるので、無駄に動作する回路が無くなり、画像符号化装置の低消費電力化を図ることができる。特に、携帯型の情報通信端末を開発する際に利点が大である。また、バスの数を増加することにより、並列化する符号化処理エレメントの数を増加することができる。さらに、有効ブロック数を算出して、処理量が少ない場合には、クロック周波数を低くすることにより、消費電力を少なくする。この場合には、伝送速度が遅いシステムあるいは画素数が少ないシステムに有効である。

【0008】

【実施例】以下、本発明の前提となる動画像符号化方式の説明、および本発明の実施例を図面により詳細に説明する。図3は、本発明の前提となるTV電話の動画像符号化方式（国際標準規格のH.261）の一例図である。ここで、入力画像20は、例えばカメラからの出力画像信号である。入力画像20は符号化フレームメモリ（以下、FM）17に取り込まれて、1画像ブロック単位（8画素×8ラインまたは16画素×16ライン）毎に有効無効・INTRA/INTER判定回路11で参照フレームメモリ（以下、FM）6に格納されている参照画像22（一つ前のフレームの符号化後、復号化された画像信号）と比較され

る。すなわち、有効無効・INTRA/INTER判定回路１１には、符号化FM１７を介して直接、現画像２７が入力されるとともに、参照もFM６からの参照画像２２が入力されて、有効／無効およびINTRA（フレーム内符号化）/INTER（フレーム間符号化）が判定される。比較された結果、二つの画像の差分が特定のしきい値より小さい時には、同じ画像（動きの無い画像）とみなされて無効ブロックと判定され、またしきい値より大きい時には有効ブロックと判定される。

【０００９】次に、無効ブロックと有効ブロックの処理手順を説明する。無効ブロックの場合には、参照フレーム（参照画像２２）と符号化フレーム（現画像２７）の画像データが等しいことにより、受信側に画像データを伝送する必要がないので、可変長符号化回路５からは単に無効ブロックであるという情報を伝送する。これに対して、有効の場合には、INTRA（フレーム内符号化）/INTER（フレーム間符号化）を判定する。INTRAは一つ前のフレームとの相関がない場合であり、現画像２７そのものを符号化し伝送する。例えば、TV放送の場合、放送画像の次にコマーシャル画像が挿入されて、全く相関がない画像になったとき等がこれに相当する。これに対して、INTERは一つ前のフレームと相関がある場合であり、例えば、TV放送の場合、同一放送のある画像と次の画像を比較した場合にこれに相当する。この場合には、現画像２７と参照画像２２との差分を取って、その差分信号を符号化し伝送する。INTERとINTRAの判定は、現画像２７と参照画像２２の相関があるか否かで決定される。しかし、同じ位置の画像だけでなく、現画像２７が参照画像２２に対して動いている場合にも、符号化した時の情報量の少ないINTERとして扱えるように、動きベクトル検出回路８で現画像２７がどの方向に何画素動いているかを求める動きベクトル検出を行って、上下左右に数画素ずらした参照画像２２と現画像２７を比較することにより、画像の動き方向を予測する。すなわち、動きを検索して、一致した位置が原点に対してどの程度動いているかを抽出する。この時、最も相関の高かった位置を動きベクトル２３とする。この動きベクトルの位置での差分が特定のしきい値よりも小さいときにINTER（フレーム間符号化）となり、またしきい値より大きい場合、すなわち相関が無い場合にINTRA（フレーム内符号化）となる。

【００１０】INTRA（フレーム内符号化）の場合には、有効無効・INTRA/INTER判定回路１１によりセレクタ１２を制御することにより、現画像２７を選択してＤＣＴ（Discrete Cosine Transform)(離散コサイン変換)回路１４でＤＣＴ処理した後、量子化回路１５で量子化し、可変長符号化回路５で可変長符号化して伝送する。さらに、逆量子化回路３で逆量子化した画像をＩＤＣＴ回路４で逆DCTし、加算回路１６を通過して参照FM６に書き込む。INTER（フレーム間符号化）の場合には、加算回路１３に符号化画像２７を入力するとともに、その符号化画像に最も相関のあった参照画像を参照FM６から動き補償回路７とローパスフィルタ（ＬＰＦ）９を通過した画像を入力して、差分とり、ＤＣＴ回路１４でＤＣＴし、量子化回路１５で量子化した後、可変長符号化回路５で可変長符号化して伝送する。同時に、参照フレームの動きベクトル２３も、可変長符号化回路５に入力することにより、可変長符号化し伝送する。さらに、前述と同じように、逆量子化した画像を逆ＤＣＴし、差分に元の画像を加えるために、参照FM６から動作補償回路７、ＬＰＦ９を通過してセレクタ１０から加算回路１６に入力した参照画像２２を加算し、参照FM６に書き込む。この参照FM６に書き込まれた画像が、次のフレームを符号化する場合の参照画像になる。従来の並列符号化装置では、図３に示すような符号化処理を行う符号化処理エレメント全体回路を複数台並列に配置し、入力画像２０をその台数分に分割して分配し、複数の符号化処理エレメントが同時に分割した入力画像を並列処理していたので、必ず複数台分の電力を消費していた。このため、消費電力が大きくなるという問題があった。

【００１１】本発明では、画像符号化する場合に、有効ブロックと無効ブロックの処理量の違いに着目して、低消費電力化を実現するものである。すなわち、無効ブロックの場合には処理量は極めて少なく、また有効ブロックの場合には動きベクトル検索，DCT，量子化，可変長符号化，逆量子化，逆DCT等の各処理が必要となるため、処理量が多くなる。これは、１フレームの符号化に必要な処理量は、有効ブロックの数に比例することを意味している。そこで、本発明においては、１フレーム内の有効ブロック数が少ない場合には、動作する符号化処理エレメントの数を少なくし、また有効ブロック数が多い場合には、並列に動作する符号化処理エレメントの数を増加するようにする。このようにして、処理量に適応して動作させる符号化処理エレメントの数を制御するようにして、低消費電力化を図るのである。これにより、処理量が少ない場合には、動作させない符号化処理エレメントのクロックを止めたり、あるいは電源を切ったり、あるいはパワーダウンモードにして電力の消費を抑えることが可能となる。

【００１２】次に、本発明の並列符号化装置の実施例を説明する。図１は、本発明の第１の実施例を示す並列符号化装置の構成図である。本実施例の並列符号化装置は、複数の符号化FM１７-i(i=1,･･･,4)，複数台の参照FM６-i(i=1,･･･,4)，１台の有効／無効判定回路１０１，４台の符号化処理エレメント１００-i(i=1,･･･,4)，１台の符号送信回路１０２から構成されている。なお、この例では、符号化処理エレメントの数を４台で説明しているが、符号化処理エレメントの数は何台でもよく、任意の数に設定できる。符号化FM１７-i(i=1,･･･,4)は、１フレーム分の入力画像を取り込むメモリである。一

方、参照FM6-i(i=1,･･･,4)は、前述と同じように、1フレーム分の画像を符号化復号化した後に格納しておくメモリで、通常1フレーム前に復号化した画像データを格納しておくメモリである。有効／無効判定回路１０１は、符号化FM１７-i(i=1,･･･,4)への画像取り込み制御、画像ブロック毎の有効／無効判定と有効ブロック数の算出、有効ブロックの数に応じて符号化処理エレメント１００-i(i=1,･･･,4)の起動制御等を行う。符号化処理エレメント１００-i(i=1,･･･,4)は、有効／無効判定回路１０１により起動されると、符号化FM１７-i(i=1,･･･,4)の現画像２７-i(i=1,･･･,4)と参照FM6-i(i=1,･･･,4)の参照画像２２-i(i=1,･･･,4)とから画像を符号化し、符号化データ２０２-i(i=1,･･･,4)を生成して符号送信回路１０２に転送する。すなわち、符号化処理エレメント１００-iは、図3におけるＤＣＴ回路１４，量子化回路１５，逆量子化回路3，ＩＤＣＴ回路4，加算回路１３，１６を含んでいる。符号送信回路１０２は、符号化処理エレメント１００-i(i=1,･･･,4)からの符号化データを受信すると、伝送する順番に伝送インタフェースへ送信データを伝送する。ここで、２０１-ｉは、現画像２７-ｉと参照画像２２-ｉとを符号化処理エレメント１００-iに伝送するとともに、符号化処理エレメント１００-iで逆量子化、逆ＤＣＴ化された参照画像を参照FM6に伝送するためのバスであって（矢印が両方に付されている）、バス数iと符号化処理エレメント１００-iの台数はそれぞれ対応しているため、バス数iが多い程、符号化処理エレメント１００-iの台数を増加させることができる。

【００１３】図2は、図1における有効／無効判定回路の動作フローチャートである。以下に、このフローの各ステップの処理内容を説明する。先ず、ステップ３００では、特定のフレーム間隔（１／３０秒，１／１５秒，１／１０秒等）で入力画像２０を符号化FM１７-1，１７-2，１７-3，１７-4に取り込む。そして、ブロック数を初期化するために、有効ブロック数，無効ブロック数ともにクリアして0にする。次に、ステップ３０１では、ブロック単位で符号化FM１７-1内の現画像２７-1と参照FM6-1の参照画像２２-1の差分を求め、それを有効／無効判定の評価関数とする。次に、ステップ３０２では、ステップ３０１で求めた有効／無効判定の評価関数が所定のしきい値よりも小さい場合には無効と判定し、ステップ３０４に分岐する。所定のしきい値よりも大きい場合には有効と判定し、ステップ３０３へ分岐する。次に、ステップ３０３では、有効ブロック数を1歩進させる。そしてステップ３０５へ進む。一方、ステップ３０４では、無効ブロック数を1歩進させる。そしてステップ３０５に進む。次に、ステップ３０５では、全ブロックの有効／無効判定を終了していれば、ステップ３０７に進み、さもなければステップ３０６へ進む。

【００１４】ステップ３０６では、次のブロックへ処理を移す（処理ブロック番号をインクリメントする）。すなわち、ステップ３０１へ戻って再び３０１～３０５の処理を行う。一方、ステップ３０７では、有効ブロックの割合を算出する。有効ブロックが0％から２５％までの時には、ステップ３０８へ分岐する。また、有効ブロックが２６％から５０％までの時には、ステップ３０９へ分岐する。さらに、有効ブロックが５０％から７５％までの時には、ステップ３１０へ分岐する。さらに、有効ブロックが７６％から１００％までの時には、ステップ３１１へ分岐する。ステップ３０８では、有効ブロックが少ないために画像を分割せず、符号化処理エレメント１００-1を起動する。一方、ステップ３０９では、有効ブロック数がやや多いので、画像を2分割してそれらに対応させる2台の符号化処理エレメント１００-1，１００-2を起動する。一方、ステップ３１０では、有効ブロック数が多いので、画像を3分割してそれらに対応させる3台の符号化処理エレメント１００-1，１００-2，１００-3を起動する。一方、ステップ３１１では、有効ブロック数が非常に多いので、画像を4分割してそれらに対応させる4台の符号化処理エレメント１００-1，１００-2，１００-3，１００-4を起動する。次に、ステップ３１２では、1フレームの符号化処理が終了するまで待つ。終了したならば、次のフレームを符号化するためにステップ３００に分岐する。

【００１５】図4（1）（2）（3）は、具体的に1フレームの画素数が３５２画素×２８８ラインの画像を符号化する場合を例にした並列画像符号化方法の説明図である。1ブロックの単位を１６画素×１６ラインとすると、1フレーム内のブロック数は３９６ブロックである。ここで符号化処理エレメントは、符号化処理に与えられた時間（例えば1／３０秒，1／１５秒，1／１０秒）内に有効ブロック９９個の処理が可能であるとする。全ブロックの有効／無効判定結果、有効ブロック数が0％から２５％までの時、つまり有効ブロック数が９９個以下の場合には、符号化処理エレメント1個で有効ブロックの符号化復号化処理を時間内で処理することができる。有効ブロック数が２６％から５０％までの時、つまり有効ブロック数が１００個から１９８個の時には、2個の符号化処理エレメントを起動して並列処理させる。この場合に、二つの符号化処理エレメントは例えば図4の（1）に示すように、処理部分を４０１と４０２に分割して並列処理を行う。次に、有効ブロックが５１％から７５％までの時、つまり有効ブロック数が１９９個から２９７個の場合には、3個の符号化処理エレメントを起動して並列処理させる。この場合に、二つの符号化処理エレメントは例えば図4の（2）に示すように、処理部分を４０３と４０４と４０５に分割して並列処理を行う。次に、有効ブロックが７６％以上の場合には、4個の符号化処理エレメントを起動して並列処理させる。この場合に、二つの符号化処理エレメントは例え

ば図4の（3）に示すように、処理部分を406と407と408と409に分割して並列処理を行う。

【0016】図6および図7は、本発明の第2の実施例を示す並列画像符号化方法の説明図である。本実施例の原理は、並列に動作する符号化処理エレメント100-iの処理量を平均化することである。これができれば、それぞれの符号化処理エレメント100-iの処理が同時に終わるので、どの符号化処理エレメント100-iにも待ち時間がなくなり、処理効率が向上して低消費電力化につながる。これを実現するためには、各符号化処理エレメント100-iが処理する画像部分における有効ブロック数が同じになれば良い。有効／無効判定回路101で有効ブロック数を計数する場合に、有効ブロックがどの場所に片寄っているかを調べることにより、各符号化処理エレメント100-iに平均化するように画像を分割するものである。図6では、画像を2分割に分割した例を示している。すなわち、（1）と（2）では有効ブロックがほぼ中央に集っているため、601と602、および603と604に均等に分割する。（3）と（4）に示すように、有効ブロックが左隅に片寄っている場合には、分割ラインを左側に寄せて分割する。このように、本実施例では、有効ブロックが二つの分割した領域で平均化するように画面を分割して、それぞれが並列に画像符号化するようにする。分割した後は、現画像と参照画像を符号化処理エレメント100-iに分配する際に、分割された画面に合致させた画素を各符号処理エレメント100-iに伝送すればよい。図7では、画像を4分割に分割した例を示している。いずれも、有効ブロックが四つの分割した領域で平均化するように画面を分割して、それぞれが並列に画像符号化するようにする。なお、図7の（1）（2）では、それぞれ縦と横に4分割しているが、有効ブロックが楕円状に集合しているので、当然のことながら両側の分割された横幅の寸法は中央部分のそれよりも少し広い（図では幅が等しくなっている）。

【0017】図5は、本発明の第3の実施例を示す画像符号化装置のブロック図である。第3の実施例では、符号化処理エレメント100-iを並列に配置することなく、クロック周波数を制御することにより低消費電力化を実現するものである。一つの符号化処理エレメント100-1を使用するとともに、有効／無効判定回路101で有効ブロックの数を算出した結果、処理量が多い場合にはクロック制御回路500のクロック周波数を高くし、一方、処理量が少ない場合には、クロック周波数を低くして、処理に必要な最適なクロック周波数にし、消費電力を抑えるものである。この実施例の場合には、伝送速度が遅いアプリケーションや画素数が少ないアプリケーションの場合に特に有効である。なお、第3の実施例の応用として、符号化処理エレメント100-iをマイクロコンピュータで実現することにより、符号化制御をプログラム可能にし、各種アプリケーション，例えばMPEG，JPEG等の動画・静止画の符号化方式にも対応できるようにする方法がある。符号化処理エレメント100-iをマイコンで構成した場合には、消費電力も少なくかつ安価となるので、携帯情報端末として好適である。さらに、第3の実施例の別の応用として、符号化処理エレメント100-iをＤＳＰ（Digital Signal Processor)で実現することにより、符号化制御をプログラム可能にして、各種アプリケーション，例えばMPEG，JPEG等の動画・静止画の符号化方式にも対応できるようにする方法がある。ＤＳＰの場合には、積和演算を得意とするので、処理速度も速く高速な画像符号化が可能である。さらに、第3の実施例の別の応用として、符号化処理エレメント100-i，有効／無効判定回路101，符号送信回路102をそれぞれLSIのマクロブロックとして設計し、これを1チップ化したLSIにする方法がある。マクロブロックとは、LSIを製造するとき、普通はそれぞれ単独に設計するのであるが、この場合には予め決定されている設計を単にはり付けるだけで製造することができるものを言う。このようにマクロブロックでLSI化することにより、特に携帯端末に実装する場合に利点が大きい。なお、本発明は、情報通信端末装置に限定するものではなく、家庭用電気製品，ゲーム等、電池やバッテリーで動作する装置に適用可能である。

【0018】

【発明の効果】以上説明したように、本発明によれば、情報通信端末装置に実装する画像符号化装置で画像の符号化・復号化を行う場合、処理量が多い有効ブロックの割合に応じて複数の符号化処理エレメントの中から必要な符号化処理エレメントを選択して起動させるので、画像符号化装置の低消費電力化を図ることができる。また、符号化の処理量が多いときにはクロック周波数を高くし、処理量が少ないときにはクロック周波数を低くして、最適なクロック周波数にすることにより、伝送速度が遅いアプリケーションや画素数の少ないアプリケーションに特に有効となり、携帯型の情報通信端末を開発する場合にその効果が大きい。

【図面の簡単な説明】

【図1】本発明の第1の実施例を示す画像符号化装置の構成図である。

【図2】本発明の一実施例を示す符号化アルゴリズムのフローチャートである。

【図3】従来の国際標準規格（H.261）の一般的な画像符号化装置の構成図である。

【図4】本発明の並列処理の処理分担を説明する図である。

【図5】本発明の第3の実施例を示す画像符号化装置の構成図である。

【図6】本発明の第2の実施例を示す並列画像符号化装置の構成図であって、二つの符号化処理エレメントで符

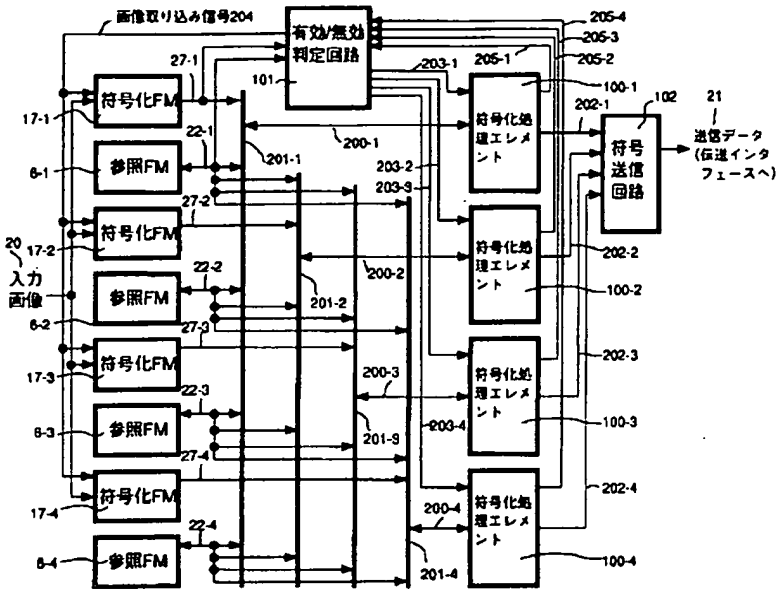
号化処理を平均化する場合の処理分担を説明するものである。

【図7】同じく第2の実施例を示す並列画像符号化装置の構成図であって、四つの符号化処理エレメントで符号化処理を平均化する場合の処理分担を説明するものである。

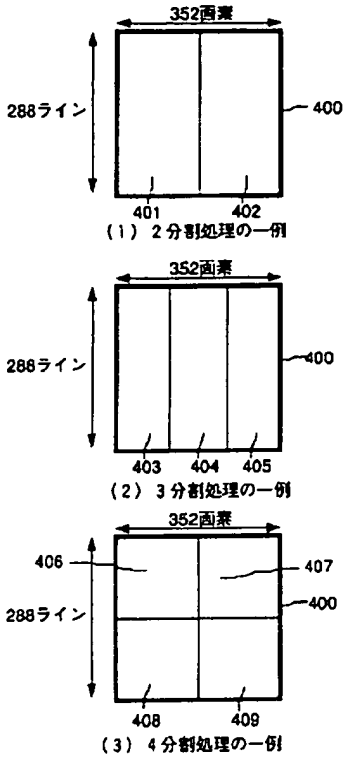
＊【符号の説明】

100-i…符号化処理エレメント、101…有効／無効判定回路、102…符号送信回路、17-i…符号化フレームメモリ、200-i…画像符号化復号化信号、201-i…信号バス、6-i…参照フレームメモリ、500…クロック制御回路。

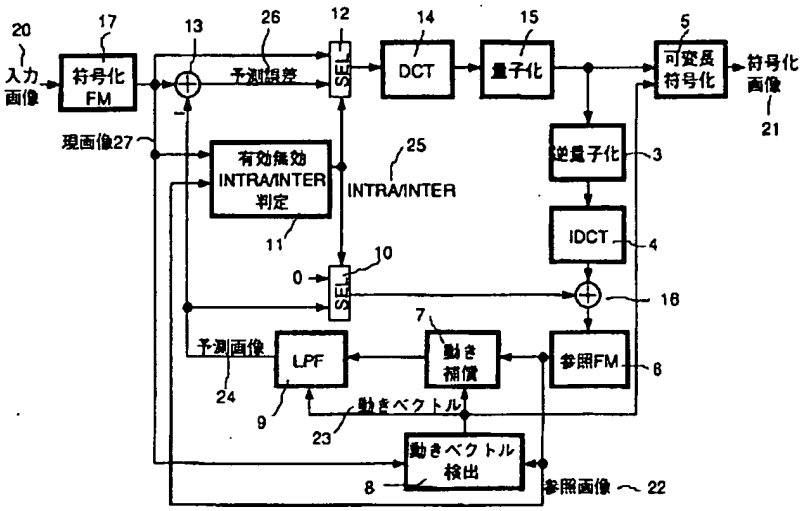
【図1】



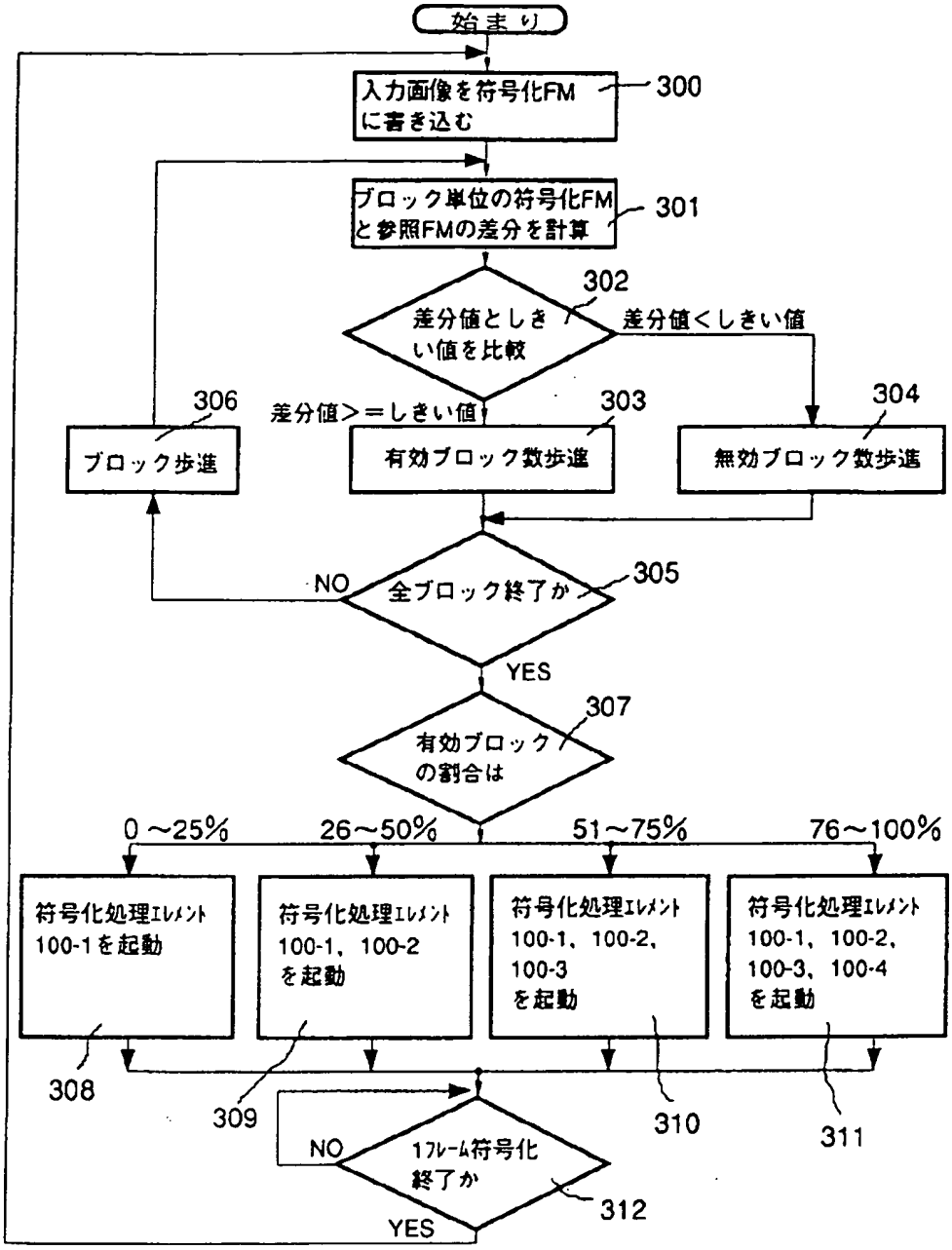
【図4】



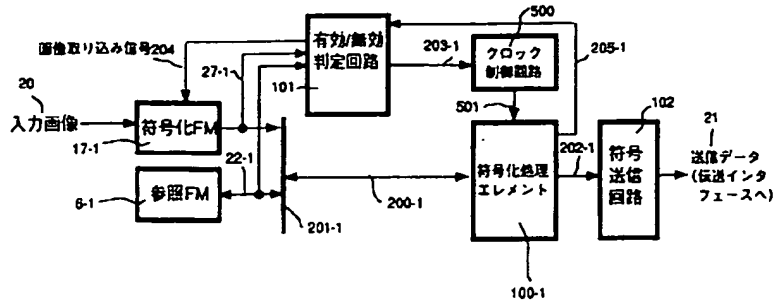
【図3】



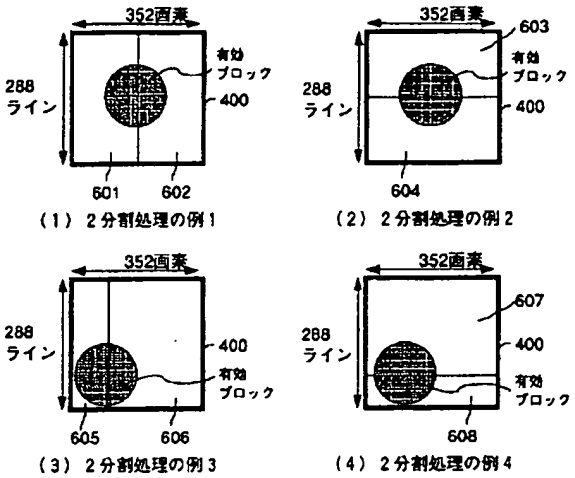
【図2】


始まり
入力画像を符号化FMに書き込む
300
ブロック単位の符号化FMと参照FMの差分を計算
301
差分値としきい値を比較
302
差分値<しきい値
差分値>＝しきい値
303
304
306
ブロック歩進
有効ブロック数歩進
無効ブロック数歩進
NO
全ブロック終了か
305
YES
有効ブロックの割合は
307
0～25%
26～50%
51～75%
76～100%
符号化処理ｴﾚﾒﾝﾄ100-1を起動
符号化処理ｴﾚﾒﾝﾄ100-1、100-2を起動
符号化処理ｴﾚﾒﾝﾄ100-1、100-2、100-3を起動
符号化処理ｴﾚﾒﾝﾄ100-1、100-2、100-3、100-4を起動
308
309
310
311
NO
1ﾌﾚｰﾑ符号化終了か
312
YES

【図5】



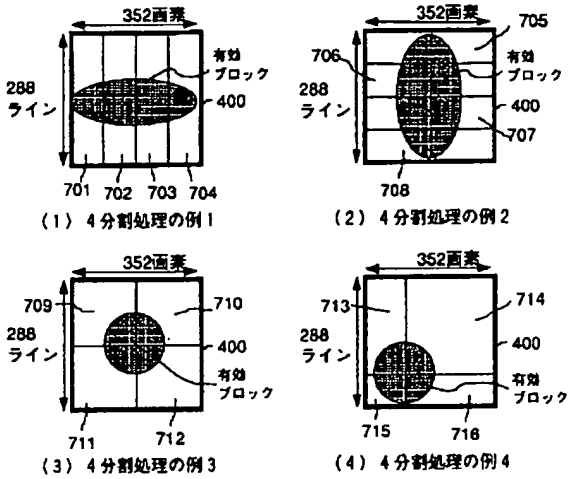
【図6】



（1）2分割処理の例1　（2）2分割処理の例2

（3）2分割処理の例3　（4）2分割処理の例4

【図7】



（1）4分割処理の例1　（2）4分割処理の例2

（3）4分割処理の例3　（4）4分割処理の例4

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-009251
(43)Date of publication of application : 10.01.1997

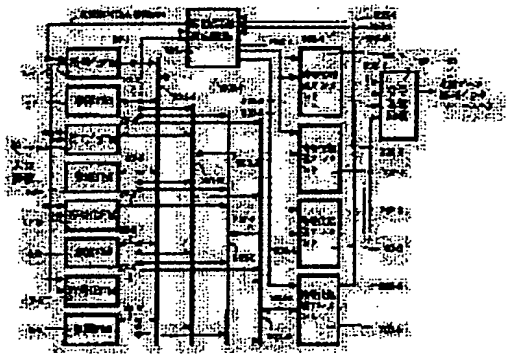
(51)Int.Cl. H04N 7/24

(21)Application number : 07-152860
(22)Date of filing : 20.06.1995

(71)Applicant : HITACHI LTD
(72)Inventor : SHIMURA TAKANORI
KATO JUNICHI

(54) PARALLEL PICTURE ENCODING METHOD AND DEVICE THEREFOR

(57)Abstract:
PURPOSE: To reduce power consumption in the case of encoding dynamic images.
CONSTITUTION: An image encoding device for encoding the dynamic images is provide with a valid/invalid judgement circuit 101 for storing the result of judging whether respective image blocks in one screen are valid or invalid and plural encoding processing elements 100-i for performing an encoding processing corresponding to the number of the valid blocks within one screen calculated in the valid/invalid judgement circuit 101. Then, the required encoding processing element 100-i is selected and activated from the plural encoding processing elements corresponding to the ratio of the valid blocks for which a processing amount is large.



CLAIMS

[Claim(s)]
[Claim 1]A parallel image encoding apparatus comprising:
A reference image memory means which stores an image comparison by which coding decryption was carried out before one.
Invalid processing to an invalid block which takes difference for every specific pixel unit block, and does not have a motion for this every pixel unit block according to a size of this difference in this image comparison and a current image coded next.
Effective/invalid judging means which changes an encoding method into effective processing to a valid block with a motion.
Two or more encoding processing means which divide a current image with a seizing signal from this effective/invalid judging means and in which each carries out coding decryption in parallel, and a numerals transmitting means which controls transmitting order of coded data which is an output from an image coding processing means of this plurality.

[Claim 2]While coding this current image from two pictures, an image comparison and a current image, In an encoding method of video which creates an image comparison required for coding of the following picture, A parallel image encoding method which computes the number of valid blocks in 1 screen, raises the degree of parallel of coding processing when a ratio of this valid block to a block of the whole ready one is high, and is characterized by making it lower the degree of parallel of coding processing when a ratio of this valid block is small.
[Claim 3]A parallel image encoding apparatus constituting said effective/invalid judging means, an encoding processing means, and a numerals transmitting means from an integrated circuit in the image encoding apparatus according to claim 1.
[Claim 4]While raising the degree of parallel of said coding processing or making it fall in the image encoding method according to claim 2, A current image is divided into plurality so that the number whose ratio of a valid block assigned to each encoding processing means is the same when dividing a current image and coding in parallel may be approached, A parallel image encoding method distributing a picture divided, respectively to each encoding processing means, and coding in parallel by each encoding processing means.
[Claim 5]An image encoding apparatus comprising:
A referred data memory measure which stores an image comparison by which coding decryption was carried out before one.
Invalid processing to an invalid block which takes difference for every specific pixel unit block, and does not have a motion for this every pixel unit block according to a size of this difference in this image comparison and a current image coded next.
Effective/invalid judging means which changes an encoding method into effective processing to a valid block with a motion.
A clock control means to control an operation clock according to valid block number information from this effective/invalid judging means, and an image coding processing means to operate with a clock from this clock control means.

[Claim 6]While coding this current image from two pictures, an image comparison and a current image, In an encoding method of video which creates an image comparison required for coding of the following picture, compute the number of valid blocks in 1 screen, and when a ratio of a valid block is high, An image encoding method which makes a clock frequency of an encoding processing circuit high, and is

characterized by lowering a clock frequency of this encoding processing circuit when a ratio of a valid block is small.

[Claim 7]A parallel image encoding apparatus constituting said encoding processing means from a microcomputer in the parallel image encoding apparatus according to claim 1.

[Claim 8]A parallel image encoding apparatus constituting said encoding processing means from a digital signal processor in the parallel image encoding apparatus according to claim 1.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]In image encoding methods, such as a television (following TV) telephone which transmits the picture compressed using the digital circuit and the wireless circuit, and a teleconference, this invention relates to a parallel image encoding method with little power consumption, and its device.
[0002]
[Description of the Prior Art]Generally the piece dropping method is conventionally known widely as an image encoding method. The usual television signal (NTSC signal) two pieces from the transmitting side to transmitting by per second 30 frames (60 field) in the piece dropping method. For example, it is the method of transmitting only one of the two in the two fields, and transmitting by per second 30 pieces, or thinning out the above-mentioned piece field further and transmitting by per second 15 or less pieces. In the receiver, reduction of the signal quantity which should be transmitted is enabled by **(ing) the transmitted same piece the first half of the two or more inning. For example, although it has sent by 30 sheets - 60 sheets in 1 second and does not sense in human being's eyes as piece dropping in TV broadcast, when it is restricted to the capacity of a transmission line like a telephone line and only ten sheets - 15 sheets can be sent in 1 second, he feels uncomfortable to human being's eyes. However, like the teleconference or TV telephone, when the movement quantity of a photographic subject is comparatively small, even if it enforces the piece dropping method, I am experimentally known [small] about sense of incongruity. In addition, it is becoming possible to carry out high efficiency coding of the picture signal, and to transmit it by signal processing, such as "orthogonal transformation, such as a discrete cosine transform,", "quantization", "inter frame prediction", and "motion compensation inter frame prediction." In this, simple inter frame prediction and motion compensation inter frame prediction are the methods of carrying out prediction coding of the following frame with reference to the frame signal coded immediately before. If such coding modes and orthogonal transformation are combined, since large relative redundancy compression is attained, it is adopted also with the video coding mode (H.261) advised in ITU-T (old CCITT: Consulting Committee of International Telegraph & Telephone).
[0003]When realizing the image encoding apparatus of an above-mentioned video coding mode, the access speed of a transmission line influences greatly. it being expectable that the coding decryption of the quality (a motion -- quick) picture can be carried out, since there is much amount of information which can be transmitted when a transmission line is a high speed (for example, transfer rate 1.5Mbps), but. To, develop the expensive hardware which can realize high speed processing of 30 frames in 1 second on the other hand is needed. On the other hand, since there is little amount of information which can be transmitted when a transmission line is a low speed (for example, transfer rate of 64k bps), although image quality deteriorates (they are [a piece dropping picture with a late motion, and] 5-15 frames in 1 second), it becomes possible to realize by low price hardware. So, when separate hardware is developed according to access speed, development cost will start with a natural thing. It becomes possible to reduce development cost substantially by realizing hardware which can be applied even when access speed is high-speed and in which parallel processing is possible, as one hardware which operates after all when a low speed [access speed] is developed, two or more these is arranged and parallel processing is carried out.
[0004]
[Problem(s) to be Solved by the Invention]As an image encoding apparatus which realizes the conventional parallel processing, there is "image encoding apparatus" indicated, for example to JP,5-304663,A. Emphasis was put on improving image quality also in a parallel processing system till then. However, when parallelizing an image encoding apparatus, the increase in the power consumption by

parallelization of an arithmetic processing unit poses a problem. Especially in the case of a portable system, in order to make it operate with a cell or a battery, the improvement about power consumption is indispensable. There is the purpose of this invention in providing a parallel image encoding method with as much as possible little power consumption, and its device, when solving such a conventional technical problem, transmitting a picture at a portable information terminal and carrying out coding decryption of the picture.

[0005]

[Means for Solving the Problem]For a ****** reason, the above-mentioned purpose in a parallel image encoding method of this invention. ** even -- correlation to every [which is a specific pixel unit about image data (image comparison) by which coding decryption was carried out before, and image data (current image) coded next] block (for example, 8 pixels x eight lines), [take and] When correlation is small, regard it as an invalid block without a motion, on the other hand, when correlation is large, regard it as a valid block with a motion, and the number of valid blocks in 1 screen is computed, One screen is divided into two or more fields when there are many valid blocks with many throughputs, Low power consumption is attained by operating a divided encoding processing circuit which performs coding processing for every field, and lessening division of one screen (or it is not necessary to divide), and lessening the number of divided encoding processing circuits which are operated for every field, when there are few valid blocks. Take correlation for every specific block, when correlation is small, consider that ** image comparison and a current image are invalid blocks without a motion, but. When correlation is large, regard it as a valid block with a motion, and the number of valid blocks in 1 screen is computed, When dividing a picture of one screen according to the number of valid blocks and coding in parallel, as a picture which divided a picture of one screen so that the number with same ratio of a valid block in a divided field might be approached, and was divided, respectively is coded in parallel, low power consumption is attained.

[0006]Take correlation for every block, in a parallel image encoding method of this invention, when correlation is small, consider that ** image comparison and a current image are invalid blocks without a motion, and it is regarded as a valid block which has a motion when correlation is large, The number of valid blocks in 1 screen is computed, and a clock frequency of an encoding processing circuit which performs coding processing when a ratio of a valid block is high is made high, and in being small, it attains low power consumption by making it lower a clock frequency of an encoding processing circuit. Low power consumption is attained by realizing **, thus an encoding processing circuit which arranges in parallel and is operated with a microcomputer of low power consumption. **, thus an encoding processing circuit which arranges in parallel and is operated are realized by a digital signal processor with quick working speed. 1 chip making of this is carried out by designing effective/invalid decision circuit which judges ** effective / invalidity, two or more encoding processing circuits which code in parallel, and a numerals sending circuit which chooses and transmits data coded in these encoding processing circuits as a macro block of LSI, respectively.

[0007]

[Function]In this invention, when the image encoding apparatus mounted in an information-and-telecommunications terminal unit performs coding and decryption of a picture, according to the rate of a valid block with many throughputs, an encoding processing circuit required for a throughput is chosen from two or more encoding processing circuits, and this is started and is operated.

Therefore, the circuit which operates vainly is lost and low power consumption of an image encoding apparatus can be attained.

An advantage is size when developing a portable information-and-telecommunications terminal especially. The number of the coding process elements to parallelize can be increased by increasing the number of buses. Power consumption is lessened by computing the number of valid blocks, and making a clock frequency low, when there are few throughputs. In this case, it is effective in a system with slow access speed, or a system with few pixel numbers.

[0008]

[Example]Hereafter, a drawing explains in detail the example of explanation of the video coding mode which will be the requisite for this invention, and this invention. Drawing 3 is an example figure of the video coding mode (H.261 of the International Standard) of TV telephone which will be the requisite for this invention. Here, the inputted image 20 is an output image signal from a camera, for example. The inputted image 20 is incorporated into the coding frame memory (following, FM) 17, it is compared with the image comparison 22 (even -- the picture signal decrypted after coding of a front frame) stored in the reference frame memory (following, FM) 6 in effective invalidity and the INTRA/INTER decision

circuit 11 at every 1 image block unit (8 pixels x eight lines, or 16 pixels x 16 lines).Namely, in effective invalidity and the INTRA/INTER decision circuit 11. While the current image 27 is directly inputted via coding FM17, as for reference, the image comparison 22 from FM6 is inputted and effective / invalidity, and INTRA(formation of frame inner code)/INTER (interframe coding) are judged. When the difference of two pictures is smaller than a specific threshold, it is regarded as the same picture (picture without a motion), and is judged with an invalid block, and as a result of being compared, when larger than a threshold, it is judged with a valid block.

[0009]Next, the procedure of an invalid block and a valid block is explained. In the case of an invalid block, according to the image data of a reference frame (image comparison 22) and a coding frame (current image 27) being equal, since it is not necessary to transmit image data to a receiver, from the variable-length-coding circuit 5, the information that it is only an invalid block is transmitted. On the other hand, in being effective, it judges INTRA(formation of frame inner code)/INTER (interframe coding). INTRA is a case where there is no correlation with the frame in front of one, and codes and transmits current image 27 itself. For example, in the case of TV broadcast, a commercial picture is inserted in the next of a broadcasted image, and the time of becoming a picture without correlation, etc. are equivalent to this. On the other hand, INTER is a case where there are a frame in front of one and correlation, for example, in the case of TV broadcast, when a picture with the same broadcast is compared with the following picture, it is equivalent [INTER] to this. In this case, the difference of the current image 27 and the image comparison 22 is taken, and that differential signal is coded and transmitted. The judgment of INTER and INTRA is determined by whether there is any correlation of the current image 27 and the image comparison 22. However, so that it can treat as INTER with little [not only the picture of the same position but when the current image 27 is moving to the image comparison 22] amount of information when it codes, The motion direction of a picture is predicted by performing motion vector detection which asks for what pixel the current image 27 is running by the motion vector detection circuit 8 in which direction, and comparing the image comparison 22 and the current image 27 which were shifted several pixels vertically and horizontally. That is, it is extracted how much a motion is searched and the congruous positions are moving to the starting point. Let the position which was the highest as for correlation be the motion vector 23 at this time. When the difference in the position of this motion vector is smaller than a specific threshold, it is set to INTER (interframe coding), and it is set to INTRA (formation of a frame inner code) when larger than a threshold (i.e., when there is no correlation).

[0010]In INTRA (formation of a frame inner code), By controlling the selector 12 by effective invalidity and the INTRA/INTER decision circuit 11, After choosing the current image 27 and carrying out DCT processing in the DCT (Discrete Cosine Transform) (discrete cosine transform) circuit 14, it quantizes in the quantization circuit 15, and variable length coding is carried out and it transmits in the variable-length-coding circuit 5. Reverse DCT of the picture which carried out inverse quantization in the inverse quantizing circuit 3 is carried out in the IDCT circuit 4, and it passes through the adder circuit 16, and writes in reference FM6. In INTER (interframe coding),While inputting the coded image 27 into the adder circuit 13, the picture which passed the reference FM6 lost-motion compensating circuit 7 and the low pass filter (LPF) 9 for the image comparison which had correlation most is inputted into the coded image, It takes by a difference and DCT is carried out in DCT circuit 14, and after quantizing in the quantization circuit 15, variable length coding is carried out and it transmits in the variable-length-coding circuit 5. Simultaneously, by inputting into the variable-length-coding circuit 5, variable length coding also of the motion vector 23 of a reference frame is carried out, and it is transmitted. In order to carry out reverse DCT of the picture which carried out inverse quantization like the above-mentioned and to add the original picture to difference, the image comparison 22 which passed of operation compensating-circuit 7 and LPF9 from reference FM6, and was inputted into the adder circuit 16 from the selector 10 is added, and it writes in reference FM6. The picture written in this reference FM6 turns into an image comparison in the case of coding the following frame. The coding process element entire circuit which performs coding processing as shown in drawing 3 in the conventional parallel encoding device is arranged to two or more set parallel, The inputted image 20 was divided into a part for the number, and was distributed, and since parallel processing of the inputted image which two or more coding process elements divided simultaneously was carried out, the electric power for two or more sets was always consumed. For this reason, there was a problem that power consumption became large.

[0011]In this invention, when carrying out image coding, low power consumption is realized paying attention to the difference in the throughput of a valid block and an invalid block. That is, in the case of an invalid block, there are very few throughputs, and since each processing of motion vector search,

DCT, quantization, variable length coding, inverse quantization, reverse DCT, etc. is needed in the case of a valid block, a throughput increases. The throughput which needs this for coding of one frame means being proportional to the number of valid blocks. So, when there are few valid blocks in one frame, it is made to increase the number of the coding process elements which lessen the number of the coding process elements which operate, and operate in parallel when there are many valid blocks in this invention. Thus, as the number of the coding process elements which are adapted for a throughput and operate it is controlled, low power consumption is attained. Thereby, when there are few throughputs, it becomes possible to stop the clock of the coding process element which is not operated, or to turn off the power, or to set it in power down mode and to hold down consumption of electric power.

[0012]Next, the example of the parallel encoding device of this invention is described. Drawing 1 is a lineblock diagram of the parallel encoding device in which the 1st example of this invention is shown. The parallel encoding device of this example Two or more coding FM17-i (i= 1, ..., 4), It comprises two or more sets of the one set of reference FM6-i (i= 1, ..., 4), coding process element of one effective/invalid decision circuit [101 or 4] 100-i (i= 1, ..., 4), and the numerals sending circuit 102. In this example, although four sets explain the number of coding process elements, may the number of coding process elements be how many, and can be set as arbitrary numbers. Coding FM17-i (i= 1, ..., 4) is a memory which incorporates the inputted image for one frame. On the other hand, reference FM6-i (i= 1, ..., 4) is a memory stored like the above-mentioned after carrying out coding decryption of the picture for one frame, and is a memory which stores the image data usually decrypted one frame ago. Effective/invalid decision circuit 101 performs start control of coding process element 100-i (i= 1, ..., 4), etc. according to the image taking control to coding FM17-i (i= 1, ..., 4), effective/invalid judging for every image block and calculation of the number of valid blocks, and the number of valid blocks. Coding process element 100-i (i= 1, ..., 4), If effective/invalid decision circuit 101 starts, a picture will be coded from current image 27-[of coding FM17-i (i= 1, ..., 4)] i (i= 1, ..., 4), and image comparison 22-[of reference FM6-i (i= 1, ..., 4)] i (i= 1, ..., 4), Coding data 202-i (i= 1, ..., 4) is generated, and it transmits to the numerals sending circuit 102. That is, coding process element 100-i includes DCT circuit 14 in drawing 3, the quantization circuit 15, the inverse quantizing circuit 3, the IDCT circuit 4, and the adder circuits 13 and 16. The numerals sending circuit 102 will transmit send data to the turn to transmit to a transmission interface, if the coding data from coding process element 100-i (i= 1, ..., 4) is received. While 201-i transmits current image 27-i and image comparison 22-i to coding process element 100-i, here, It is a bus for transmitting inverse quantization and the image comparison formed into reverse DCT to reference FM6 by coding process element 100-i (the arrow is given to both), They can make the number of coding process element 100-i increase, so that there are many buses i, since the number i of buses and the number of coding process element 100-i correspond, respectively.

[0013]Drawing 2 is an operation flow chart of effective/invalid decision circuit in drawing 1. Below, the contents of processing of each step of this flow are explained. First, in Step 300, the inputted image 20 is incorporated into coding FM17-1,17-2 and 17-3,17-4 with specific frame intervals (1 / 30 seconds, 15 1/seconds, 10 etc. 1/seconds, etc.). And since the block count is initialized, the number of valid blocks and the number of invalid blocks are cleared, and it is made 0. Next, in Step 301, it asks for the difference of the current image 27-1 in coding FM17-1, and the image comparison 22-1 of reference FM6-1 by a block unit, and let it be a valuation function of effective/invalid judging. Next, in Step 302, when the valuation function of effective/invalid judging for which it asked at Step 301 is smaller than a predetermined threshold, it judges with it being invalid, and it branches to Step 304. In being larger than a predetermined threshold, it judges with it being effective, and it branches to Step 303. Next, in Step 303, 1 stepping of the number of valid blocks is carried out. And it progresses to Step 305. On the other hand, in Step 304, 1 stepping of the number of invalid blocks is carried out. And it progresses to Step 305. Next, in Step 305, if effective/invalid judging of a whole block is ended, it will progress to Step 307, otherwise will progress to Step 306.

[0014]In Step 306, processing is moved to the following block (a processing block number is **********ed). That is, it returns to Step 301 and 301-305 are processed again. On the other hand, the rate of a valid block is computed in Step 307. When a valid block is from 0% to 25%, it branches to Step 308. When a valid block is from 26% to 50%, it branches to Step 309. When a valid block is from 50% to 75%, it branches to Step 310. When a valid block is from 76% to 100%, it branches to Step 311. In Step 308, since there are few valid blocks, a picture is not divided, but the coding process element 100-1 is started. On the other hand, in Step 309, since there are slightly many valid blocks, two-set process element [of coding] 100-1,100-2 which divides a picture into two and is made to correspond to them is started. On the other hand, in Step 310, since there are many valid blocks, three sets of coding process

element 100-1,100-2,100-3 which trichotomizes a picture and is made to correspond to them are started. On the other hand, in Step 311, since there are dramatically many valid blocks, four-set process element [of coding] 100-1,100-2,100-3,100-4 which quadrisects a picture and is made to correspond to them is started. Next, in Step 312, it waits until coding processing of one frame is completed. If it ends, in order to code the following frame, it will branch to Step 300.

[0015]Drawing 4 (1), (2), and (3) is an explanatory view of the parallel image encoding method which made the example the case where the picture whose pixel numbers of one frame are 352 pixels x 288 lines concretely was coded. When a 1-block unit shall be 16 pixels x 16 lines, the block count in one frame is 396 blocks. A coding process element enables processing of 99 valid blocks here within the time (for example, 1 / 30 seconds, 15 1/seconds, 10 1/seconds) given to coding processing. When the number of valid blocks is 99 or less pieces when effective/invalid decision result of a whole block and the number of valid blocks are from 0% to 25% that is, the coding decoding processing of a valid block can be processed by within a time by one coding process element. When the number of valid blocks is from 26% to 50% that is, the number of valid blocks starts and carries out parallel processing of the two coding process elements at the time of 100 to 198 pieces. In this case, as shown in (1) of drawing 4, two coding process elements divide a processing part into 401 and 402, and perform parallel processing. Next, when a valid block is from 51% to 75% that is, the number of valid blocks starts and carries out parallel processing of the three coding process elements to 199 to 297 cases. In this case, as shown in (2) of drawing 4, two coding process elements divide a processing part into 403, and 404 and 405, and perform parallel processing. Next, when a valid block is not less than 76%, parallel processing of the four coding process elements is started and carried out. In this case, as shown in (3) of drawing 4, two coding process elements divide a processing part into 406, 407, and 408 and 409, and perform parallel processing.

[0016]Drawing 6 and drawing 7 are the explanatory views of a parallel image encoding method showing the 2nd example of this invention. The principle of this example is equalizing the throughput of coding process element 100-i which operates in parallel. Since processing of each coding process element 100-i will finish simultaneously if this is made, waiting time is lost to every coding process element 100-i, processing efficiency improves, and it leads to low power consumption. In order to realize this, the number of valid blocks in the image region which processes each coding process element 100-i should just become the same. When calculating the number of valid blocks in effective/invalid decision circuit 101, a picture is divided by investigating toward which place the valid block inclines so that it may equalize to each coding process element 100-i. Drawing 6 shows the example which divided the picture comparatively for 2 minutes. Namely, in (1) and (2), since valid blocks have gathered in the center mostly, it divides into 601, 602, and 603 and 604 uniformly. As it is indicated in (4) as (3), when the valid block inclines toward the left corner, a division line is brought near by left-hand side, and is divided. Thus, a screen is divided so that a valid block may equalize in two divided fields, and in this example, each is made to carry out image coding in parallel. What is necessary is just to transmit the pixel which made the divided screen agree to each numerals process element 100-i, when distributing a current image and an image comparison to coding process element 100-i after dividing. Drawing 7 shows the example which divided the picture into quadrisection. All divide a screen so that a valid block may equalize in four divided fields, and each is made to carry out image coding in parallel. Although quadrisected length and horizontally, respectively, since valid blocks have gathered in the shape of an ellipse, the size of the breadth into which both sides were divided with the natural thing is somewhat larger than that of a center portion at (1) of drawing 7, and (2) (by a diagram, width is equal).

[0017]Drawing 5 is a block diagram of the image encoding apparatus in which the 3rd example of this invention is shown. In the 3rd example, low power consumption is realized by controlling a clock frequency, without arranging coding process element 100-i in parallel. The result of having computed the number of valid blocks in effective/invalid decision circuit 101 while using the one coding process element 100-1, When there are many throughputs, the clock frequency of the clock control circuit 500 is made high, on the other hand, when there are few throughputs, a clock frequency is made low, it is made the optimal clock frequency required for processing, and power consumption is stopped. In the case of this example, it is effective especially when it is application with slow access speed, and application with few pixel numbers. As application of the 3rd example, by realizing coding process element 100-i with a microcomputer, encoding control is made programmable and there is the method of enabling it to correspond also to the coding mode of an animation and still pictures, such as various applications, for example, MPEG, and JPEG. Since it becomes there is also little power consumption and cheap [power consumption] when coding process element 100-i is constituted from a microcomputer,

it is suitable as a Personal Digital Assistant. By realizing coding process element 100-i by DSP (Digital Signal Processor) as another application of the 3rd example, Encoding control is made programmable and there is the method of enabling it to correspond also to the coding mode of an animation and still pictures, such as various applications, for example, MPEG, and JPEG. In the case of DSP, since product sum operation is made elated, high-speed quick image coding is possible also for processing speed. As another application of the 3rd example, coding process element 100-i, effective/invalid decision circuit 101, and the numerals sending circuit 102 are designed as a macro block of LSI, respectively, and there is the method of setting to LSI which carried out 1 chip making of this. A macro block is independently designed usually, respectively, when manufacturing LSI, but it means what can be manufactured only by sticking the design for which it opts beforehand in this case. Thus, by LSI-izing by a macro block, when it mounts especially in a personal digital assistant, an advantage is large. This invention cannot be limited to an information-and-telecommunications terminal unit, and can apply a home appliance, a game, etc. to the device which operates with a cell or a battery.

[0018]

[Effect of the Invention]As explained above, when the image encoding apparatus mounted in an information-and-telecommunications terminal unit performs coding and decryption of a picture, in this invention, a required coding process element is chosen and started out of two or more coding process elements according to the rate of a valid block with many throughputs.

Therefore, low power consumption of an image encoding apparatus can be attained.

By making a clock frequency high, when there are many throughputs of coding, making a clock frequency low, when there are few throughputs, and making it the optimal clock frequency, The effect is large, when becoming especially effective in application with slow access speed, or application with few pixel numbers and developing a portable information-and-telecommunications terminal.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application]In image encoding methods, such as a television (following TV) telephone which transmits the picture compressed using the digital circuit and the wireless circuit, and a teleconference, this invention relates to a parallel image encoding method with little power consumption, and its device.

[Translation done.]

* NOTICES *

PRIOR ART

[Description of the Prior Art]Generally the piece dropping method is conventionally known widely as an image encoding method. The usual television signal (NTSC signal) two pieces from the transmitting side to transmitting by per second 30 frames (60 field) in the piece dropping method. For example, it is the method of transmitting only one of the two in the two fields, and transmitting by per second 30 pieces, or thinning out the above-mentioned piece field further and transmitting by per second 15 or less pieces. In the receiver, reduction of the signal quantity which should be transmitted is enabled by **(ing) the transmitted same piece the first half of the two or more inning. For example, although it has sent by 30 sheets - 60 sheets in 1 second and does not sense in human being's eyes as piece dropping in TV broadcast, when it is restricted to the capacity of a transmission line like a telephone line and only ten sheets - 15 sheets can be sent in 1 second, he feels uncomfortable to human being's eyes. However, like the teleconference or TV telephone, when the movement quantity of a photographic subject is comparatively small, even if it enforces the piece dropping method, I am experimentally known [small] about sense of incongruity. In addition, it is becoming possible to carry out high efficiency coding of the picture signal, and to transmit it by signal processing, such as "orthogonal transformation, such as a discrete cosine transform,", "quantization", "inter frame prediction", and "motion compensation inter frame prediction." In this, simple inter frame prediction and motion compensation inter frame prediction are the methods of carrying out prediction coding of the following frame with reference to the frame signal coded immediately before. If such coding modes and orthogonal transformation are combined, since large relative redundancy compression is attained, it is adopted also with the video coding mode (H.261) advised in ITU-T (old CCITT: Consulting Committee of International Telegraph & Telephone). [0003]When realizing the image encoding apparatus of an above-mentioned video coding mode, the access speed of a transmission line influences greatly. it being expectable that the coding decryption of the quality (a motion -- quick) picture can be carried out, since there is much amount of information which can be transmitted when a transmission line is a high speed (for example, transfer rate 1.5Mbps), but. To, develop the expensive hardware which can realize high speed processing of 30 frames in 1 second on the other hand is needed. On the other hand, since there is little amount of information which can be transmitted when a transmission line is a low speed (for example, transfer rate of 64k bps), although image quality deteriorates (they are [a piece dropping picture with a late motion, and] 5-15 frames in 1 second), it becomes possible to realize by low price hardware. So, when separate hardware is developed according to access speed, development cost will start with a natural thing. It becomes possible to reduce development cost substantially by realizing hardware which can be applied even when access speed is high-speed and in which parallel processing is possible, as one hardware which operates after all when a low speed [access speed] is developed, two or more these is arranged and parallel processing is carried out.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, when the image encoding apparatus mounted in an information-and-telecommunications terminal unit performs coding and decryption of a picture, in this invention, a required coding process element is chosen and started out of two or more coding process elements according to the rate of a valid block with many throughputs.
Therefore, low power consumption of an image encoding apparatus can be attained.
By making a clock frequency high, when there are many throughputs of coding, making a clock frequency low, when there are few throughputs, and making it the optimal clock frequency, The effect is large, when becoming especially effective in application with slow access speed, or application with few pixel numbers and developing a portable information-and-telecommunications terminal.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]As an image encoding apparatus which realizes the conventional parallel processing, there is "image encoding apparatus" indicated, for example to JP,5-304663,A. Emphasis was put on improving image quality also in a parallel processing system till then. However, when parallelizing an image encoding apparatus, the increase in the power consumption by parallelization of an arithmetic processing unit poses a problem. Especially in the case of a portable system, in order to make it operate with a cell or a battery, the improvement about power consumption is indispensable. There is the purpose of this invention in providing a parallel image encoding method with as much as possible little power consumption, and its device, when solving such a conventional technical problem, transmitting a picture at a portable information terminal and carrying out coding decryption of the picture.

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem]For a ****** reason, the above-mentioned purpose in a parallel image encoding method of this invention. ** even -- correlation to every [which is a specific pixel unit about image data (image comparison) by which coding decryption was carried out before, and image data (current image) coded next] block (for example, 8 pixels x eight lines), [take and] When correlation is small, regard it as an invalid block without a motion, on the other hand, when correlation is large, regard it as a valid block with a motion, and the number of valid blocks in 1 screen is computed, One screen is divided into two or more fields when there are many valid blocks with many throughputs, Low power consumption is attained by operating a divided encoding processing circuit which performs coding processing for every field, and lessening division of one screen (or it is not necessary to divide), and lessening the number of divided encoding processing circuits which are operated for every field, when there are few valid blocks. Take correlation for every specific block, when correlation is small, consider that ** image comparison and a current image are invalid blocks without a motion, but. When correlation is large, regard it as a valid block with a motion, and the number of valid blocks in 1 screen is computed, When dividing a picture of one screen according to the number of valid blocks and coding in parallel, as a picture which divided a picture of one screen so that the number with same ratio of a valid block in a divided field might be approached, and was divided, respectively is coded in parallel, low power consumption is attained.
[0006]Take correlation for every block, in a parallel image encoding method of this invention, when correlation is small, consider that ** image comparison and a current image are invalid blocks without a motion, and it is regarded as a valid block which has a motion when correlation is large, The number of valid blocks in 1 screen is computed, and a clock frequency of an encoding processing circuit which performs coding processing when a ratio of a valid block is high is made high, and in being small, it attains low power consumption by making it lower a clock frequency of an encoding processing circuit. Low power consumption is attained by realizing **, thus an encoding processing circuit which arranges in parallel and is operated with a microcomputer of low power consumption. **, thus an encoding processing circuit which arranges in parallel and is operated are realized by a digital signal processor with quick working speed. 1 chip making of this is carried out by designing effective/invalid decision circuit which judges ** effective / invalidity, two or more encoding processing circuits which code in parallel, and a numerals sending circuit which chooses and transmits data coded in these encoding processing circuits as a macro block of LSI, respectively.

[Translation done.]

* NOTICES *

OPERATION

[Function]In this invention, when the image encoding apparatus mounted in an information-and-telecommunications terminal unit performs coding and decryption of a picture, according to the rate of a valid block with many throughputs, an encoding processing circuit required for a throughput is chosen from two or more encoding processing circuits, and this is started and is operated.
Therefore, the circuit which operates vainly is lost and low power consumption of an image encoding apparatus can be attained.
An advantage is size when developing a portable information-and-telecommunications terminal especially. The number of the coding process elements to parallelize can be increased by increasing the number of buses. Power consumption is lessened by computing the number of valid blocks, and making a clock frequency low, when there are few throughputs. In this case, it is effective in a system with slow access speed, or a system with few pixel numbers.

[Translation done.]

EXAMPLE

[Example]Hereafter, a drawing explains in detail the example of explanation of the video coding mode which will be the requisite for this invention, and this invention. Drawing 3 is an example figure of the video coding mode (H.261 of the International Standard) of TV telephone which will be the requisite for this invention. Here, the inputted image 20 is an output image signal from a camera, for example. The inputted image 20 is incorporated into the coding frame memory (following, FM) 17, it is compared with the image comparison 22 (even -- the picture signal decrypted after coding of a front frame) stored in the reference frame memory (following, FM) 6 in effective invalidity and the INTRA/INTER decision circuit 11 at every 1 image block unit (8 pixels x eight lines, or 16 pixels x 16 lines).Namely, in effective invalidity and the INTRA/INTER decision circuit 11. While the current image 27 is directly inputted via coding FM17, as for reference, the image comparison 22 from FM6 is inputted and effective / invalidity, and INTRA(formation of frame inner code)/INTER (interframe coding) are judged. When the difference of two pictures is smaller than a specific threshold, it is regarded as the same picture (picture without a motion), and is judged with an invalid block, and as a result of being compared, when larger than a threshold, it is judged with a valid block.

[0009]Next, the procedure of an invalid block and a valid block is explained. In the case of an invalid block, according to the image data of a reference frame (image comparison 22) and a coding frame (current image 27) being equal, since it is not necessary to transmit image data to a receiver, from the variable-length-coding circuit 5, the information that it is only an invalid block is transmitted. On the other hand, in being effective, it judges INTRA(formation of frame inner code)/INTER (interframe coding). INTRA is a case where there is no correlation with the frame in front of one, and codes and transmits current image 27 itself. For example, in the case of TV broadcast, a commercial picture is inserted in the next of a broadcasted image, and the time of becoming a picture without correlation, etc. are equivalent to this. On the other hand, INTER is a case where there are a frame in front of one and correlation, for example, in the case of TV broadcast, when a picture with the same broadcast is compared with the following picture, it is equivalent [INTER] to this. In this case, the difference of the current image 27 and the image comparison 22 is taken, and that differential signal is coded and transmitted. The judgment of INTER and INTRA is determined by whether there is any correlation of the current image 27 and the image comparison 22. However, so that it can treat as INTER with little [not only the picture of the same position but when the current image 27 is moving to the image comparison 22] amount of information when it codes, The motion direction of a picture is predicted by performing motion vector detection which asks for what pixel the current image 27 is running by the motion vector detection circuit 8 in which direction, and comparing the image comparison 22 and the current image 27 which were shifted several pixels vertically and horizontally. That is, it is extracted how much a motion is searched and the congruous positions are moving to the starting point. Let the position which was the highest as for correlation be the motion vector 23 at this time. When the difference in the position of this motion vector is smaller than a specific threshold, it is set to INTER (interframe coding), and it is set to INTRA (formation of a frame inner code) when larger than a threshold (i.e., when there is no correlation).

[0010]In INTRA (formation of a frame inner code), By controlling the selector 12 by effective invalidity and the INTRA/INTER decision circuit 11, After choosing the current image 27 and carrying out DCT processing in the DCT (Discrete Cosine Transform) (discrete cosine transform) circuit 14, it quantizes in the quantization circuit 15, and variable length coding is carried out and it transmits in the variable-length-coding circuit 5. Reverse DCT of the picture which carried out inverse quantization in the inverse quantizing circuit 3 is carried out in the IDCT circuit 4, and it passes through the adder circuit 16, and writes in reference FM6. In INTER (interframe coding),While inputting the coded image 27 into the adder

circuit 13, the picture which passed the reference FM6 lost-motion compensating circuit 7 and the low pass filter (LPF) 9 for the image comparison which had correlation most is inputted into the coded image, It takes by a difference and DCT is carried out in DCT circuit 14, and after quantizing in the quantization circuit 15, variable length coding is carried out and it transmits in the variable-length-coding circuit 5. Simultaneously, by inputting into the variable-length-coding circuit 5, variable length coding also of the motion vector 23 of a reference frame is carried out, and it is transmitted. In order to carry out reverse DCT of the picture which carried out inverse quantization like the above-mentioned and to add the original picture to difference, the image comparison 22 which passed of operation compensating-circuit 7 and LPF9 from reference FM6, and was inputted into the adder circuit 16 from the selector 10 is added, and it writes in reference FM6. The picture written in this reference FM6 turns into an image comparison in the case of coding the following frame. The coding process element entire circuit which performs coding processing as shown in drawing 3 in the conventional parallel encoding device is arranged to two or more set parallel, The inputted image 20 was divided into a part for the number, and was distributed, and since parallel processing of the inputted image which two or more coding process elements divided simultaneously was carried out, the electric power for two or more sets was always consumed. For this reason, there was a problem that power consumption became large.

[0011]In this invention, when carrying out image coding, low power consumption is realized paying attention to the difference in the throughput of a valid block and an invalid block. That is, in the case of an invalid block, there are very few throughputs, and since each processing of motion vector search, DCT, quantization, variable length coding, inverse quantization, reverse DCT, etc. is needed in the case of a valid block, a throughput increases. The throughput which needs this for coding of one frame means being proportional to the number of valid blocks. So, when there are few valid blocks in one frame, it is made to increase the number of the coding process elements which lessen the number of the coding process elements which operate, and operate in parallel when there are many valid blocks in this invention. Thus, as the number of the coding process elements which are adapted for a throughput and operate it is controlled, low power consumption is attained. Thereby, when there are few throughputs, it becomes possible to stop the clock of the coding process element which is not operated, or to turn off the power, or to set it in power down mode and to hold down consumption of electric power.

[0012]Next, the example of the parallel encoding device of this invention is described. Drawing 1 is a lineblock diagram of the parallel encoding device in which the 1st example of this invention is shown. The parallel encoding device of this example Two or more coding FM17-i (i= 1, ..., 4), It comprises two or more sets of the one set of reference FM6-i (i= 1, ..., 4), coding process element of one effective/invalid decision circuit [101 or 4] 100-i (i= 1, ..., 4), and the numerals sending circuit 102. In this example, although four sets explain the number of coding process elements, may the number of coding process elements be how many, and can be set as arbitrary numbers. Coding FM17-i (i= 1, ..., 4) is a memory which incorporates the inputted image for one frame. On the other hand, reference FM6-i (i= 1, ..., 4) is a memory stored like the above-mentioned after carrying out coding decryption of the picture for one frame, and is a memory which stores the image data usually decrypted one frame ago. Effective/invalid decision circuit 101 performs start control of coding process element 100-i (i= 1, ..., 4), etc. according to the image taking control to coding FM17-i (i= 1, ..., 4), effective/invalid judging for every image block and calculation of the number of valid blocks, and the number of valid blocks. Coding process element 100-i (i= 1, ..., 4), If effective/invalid decision circuit 101 starts, a picture will be coded from current image 27-[of coding FM17-i (i= 1, ..., 4)] i (i= 1, ..., 4), and image comparison 22-[of reference FM6-i (i= 1, ..., 4)] i (i= 1, ..., 4), Coding data 202-i (i= 1, ..., 4) is generated, and it transmits to the numerals sending circuit 102. That is, coding process element 100-i includes DCT circuit 14 in drawing 3, the quantization circuit 15, the inverse quantizing circuit 3, the IDCT circuit 4, and the adder circuits 13 and 16. The numerals sending circuit 102 will transmit send data to the turn to transmit to a transmission interface, if the coding data from coding process element 100-i (i= 1, ..., 4) is received. While 201-i transmits current image 27-i and image comparison 22-i to coding process element 100-i, here, It is a bus for transmitting inverse quantization and the image comparison formed into reverse DCT to reference FM6 by coding process element 100-i (the arrow is given to both), They can make the number of coding process element 100-i increase, so that there are many buses i, since the number i of buses and the number of coding process element 100-i correspond, respectively.

[0013]Drawing 2 is an operation flow chart of effective/invalid decision circuit in drawing 1. Below, the contents of processing of each step of this flow are explained. First, in Step 300, the inputted image 20 is incorporated into coding FM17-1,17-2 and 17-3,17-4 with specific frame intervals (1 / 30 seconds, 15 1/seconds, 10 etc. 1/seconds, etc.). And since the block count is initialized, the number of valid blocks

and the number of invalid blocks are cleared, and it is made 0. Next, in Step 301, it asks for the difference of the current image 27-1 in coding FM17-1, and the image comparison 22-1 of reference FM6-1 by a block unit, and let it be a valuation function of effective/invalid judging. Next, in Step 302, when the valuation function of effective/invalid judging for which it asked at Step 301 is smaller than a predetermined threshold, it judges with it being invalid, and it branches to Step 304. In being larger than a predetermined threshold, it judges with it being effective, and it branches to Step 303. Next, in Step 303, 1 stepping of the number of valid blocks is carried out. And it progresses to Step 305. On the other hand, in Step 304, 1 stepping of the number of invalid blocks is carried out. And it progresses to Step 305. Next, in Step 305, if effective/invalid judging of a whole block is ended, it will progress to Step 307, otherwise will progress to Step 306.

[0014]In Step 306, processing is moved to the following block (a processing block number is **********ed). That is, it returns to Step 301 and 301-305 are processed again. On the other hand, the rate of a valid block is computed in Step 307. When a valid block is from 0% to 25%, it branches to Step 308. When a valid block is from 26% to 50%, it branches to Step 309. When a valid block is from 50% to 75%, it branches to Step 310. When a valid block is from 76% to 100%, it branches to Step 311. In Step 308, since there are few valid blocks, a picture is not divided, but the coding process element 100-1 is started. On the other hand, in Step 309, since there are slightly many valid blocks, two-set process element [of coding] 100-1,100-2 which divides a picture into two and is made to correspond to them is started. On the other hand, in Step 310, since there are many valid blocks, three sets of coding process element 100-1,100-2,100-3 which trichotomizes a picture and is made to correspond to them are started. On the other hand, in Step 311, since there are dramatically many valid blocks, four-set process element [of coding] 100-1,100-2,100-3,100-4 which quadrisects a picture and is made to correspond to them is started. Next, in Step 312, it waits until coding processing of one frame is completed. If it ends, in order to code the following frame, it will branch to Step 300.

[0015]Drawing 4 (1), (2), and (3) is an explanatory view of the parallel image encoding method which made the example the case where the picture whose pixel numbers of one frame are 352 pixels x 288 lines concretely was coded. When a 1-block unit shall be 16 pixels x 16 lines, the block count in one frame is 396 blocks. A coding process element enables processing of 99 valid blocks here within the time (for example, 1 / 30 seconds, 15 1/seconds, 10 1/seconds) given to coding processing. When the number of valid blocks is 99 or less pieces when effective/invalid decision result of a whole block and the number of valid blocks are from 0% to 25% that is, the coding decoding processing of a valid block can be processed by within a time by one coding process element. When the number of valid blocks is from 26% to 50% that is, the number of valid blocks starts and carries out parallel processing of the two coding process elements at the time of 100 to 198 pieces. In this case, as shown in (1) of drawing 4, two coding process elements divide a processing part into 401 and 402, and perform parallel processing. Next, when a valid block is from 51% to 75% that is, the number of valid blocks starts and carries out parallel processing of the three coding process elements to 199 to 297 cases. In this case, as shown in (2) of drawing 4, two coding process elements divide a processing part into 403, and 404 and 405, and perform parallel processing. Next, when a valid block is not less than 76%, parallel processing of the four coding process elements is started and carried out. In this case, as shown in (3) of drawing 4, two coding process elements divide a processing part into 406, 407, and 408 and 409, and perform parallel processing.

[0016]Drawing 6 and drawing 7 are the explanatory views of a parallel image encoding method showing the 2nd example of this invention. The principle of this example is equalizing the throughput of coding process element 100-i which operates in parallel. Since processing of each coding process element 100-i will finish simultaneously if this is made, waiting time is lost to every coding process element 100-i, processing efficiency improves, and it leads to low power consumption. In order to realize this, the number of valid blocks in the image region which processes each coding process element 100-i should just become the same. When calculating the number of valid blocks in effective/invalid decision circuit 101, a picture is divided by investigating toward which place the valid block inclines so that it may equalize to each coding process element 100-i. Drawing 6 shows the example which divided the picture comparatively for 2 minutes. Namely, in (1) and (2), since valid blocks have gathered in the center mostly, it divides into 601, 602, and 603 and 604 uniformly. As it is indicated in (4) as (3), when the valid block inclines toward the left corner, a division line is brought near by left-hand side, and is divided. Thus, a screen is divided so that a valid block may equalize in two divided fields, and in this example, each is made to carry out image coding in parallel. What is necessary is just to transmit the pixel which made the divided screen agree to each numerals process element 100-i, when distributing a current

image and an image comparison to coding process element 100-i after dividing. Drawing 7 shows the example which divided the picture into quadrisection. All divide a screen so that a valid block may equalize in four divided fields, and each is made to carry out image coding in parallel. Although quadrisected length and horizontally, respectively, since valid blocks have gathered in the shape of an ellipse, the size of the breadth into which both sides were divided with the natural thing is somewhat larger than that of a center portion at (1) of drawing 7, and (2) (by a diagram, width is equal).

[0017]Drawing 5 is a block diagram of the image encoding apparatus in which the 3rd example of this invention is shown. In the 3rd example, low power consumption is realized by controlling a clock frequency, without arranging coding process element 100-i in parallel. The result of having computed the number of valid blocks in effective/invalid decision circuit 101 while using the one coding process element 100-1, When there are many throughputs, the clock frequency of the clock control circuit 500 is made high, on the other hand, when there are few throughputs, a clock frequency is made low, it is made the optimal clock frequency required for processing, and power consumption is stopped. In the case of this example, it is effective especially when it is application with slow access speed, and application with few pixel numbers. As application of the 3rd example, by realizing coding process element 100-i with a microcomputer, encoding control is made programmable and there is the method of enabling it to correspond also to the coding mode of an animation and still pictures, such as various applications, for example, MPEG, and JPEG. Since it becomes there is also little power consumption and cheap [power consumption] when coding process element 100-i is constituted from a microcomputer, it is suitable as a Personal Digital Assistant. By realizing coding process element 100-i by DSP (Digital Signal Processor) as another application of the 3rd example, Encoding control is made programmable and there is the method of enabling it to correspond also to the coding mode of an animation and still pictures, such as various applications, for example, MPEG, and JPEG. In the case of DSP, since product sum operation is made elated, high-speed quick image coding is possible also for processing speed. As another application of the 3rd example, coding process element 100-i, effective/invalid decision circuit 101, and the numerals sending circuit 102 are designed as a macro block of LSI, respectively, and there is the method of setting to LSI which carried out 1 chip making of this. A macro block is independently designed usually, respectively, when manufacturing LSI, but it means what can be manufactured only by sticking the design for which it opts beforehand in this case. Thus, by LSI-izing by a macro block, when it mounts especially in a personal digital assistant, an advantage is large. This invention cannot be limited to an information-and-telecommunications terminal unit, and can apply a home appliance, a game, etc. to the device which operates with a cell or a battery.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

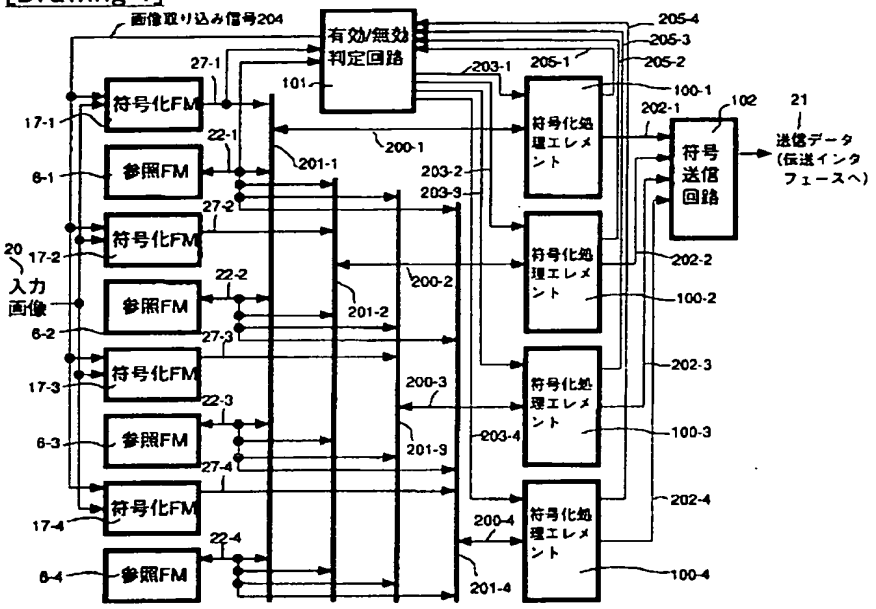
[Brief Description of the Drawings]
[Drawing 1]It is a lineblock diagram of the image encoding apparatus in which the 1st example of this invention is shown.
[Drawing 2]It is a flow chart of the encoding algorithm which shows one example of this invention.
[Drawing 3]It is a lineblock diagram of the common image encoding apparatus of the conventional International Standard (H.261).
[Drawing 4]It is a figure explaining a processing assignment of the parallel processing of this invention.
[Drawing 5]It is a lineblock diagram of the image encoding apparatus in which the 3rd example of this invention is shown.
[Drawing 6]It is a lineblock diagram of the parallel image encoding apparatus in which the 2nd example of this invention is shown, and the processing assignment in the case of equalizing coding processing by two coding process elements is explained.
[Drawing 7]It is a lineblock diagram of the parallel image encoding apparatus in which the 2nd example is similarly shown, and the processing assignment in the case of equalizing coding processing by four coding process elements is explained.
[Description of Notations]
100-i [-- A coding frame memory, 200-i / -- An image coding decoded signal, 201-i / -- A signal bus, 6-i / -- A reference frame memory, 500 / -- Clock control circuit.] -- A coding process element, 101 -- Effective/invalid decision circuit, 102 -- A numerals sending circuit, 17-i

---

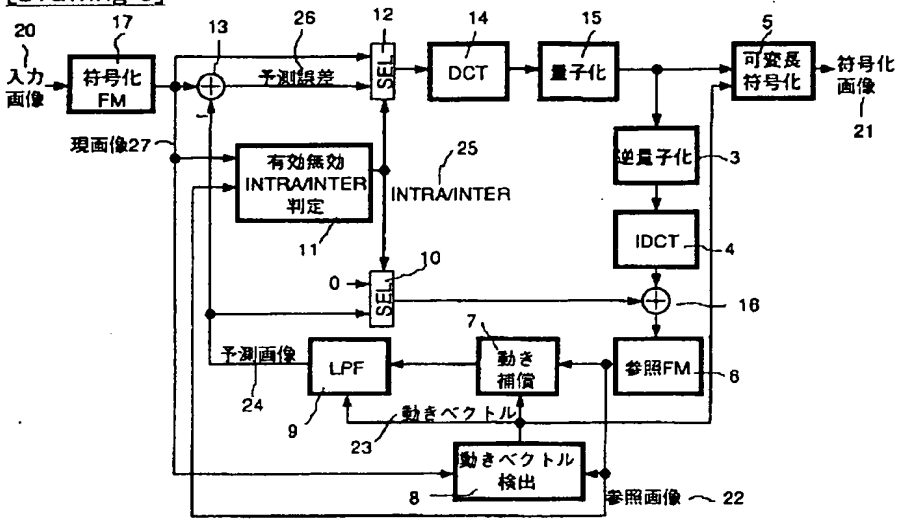
[Translation done.]

DRAWINGS

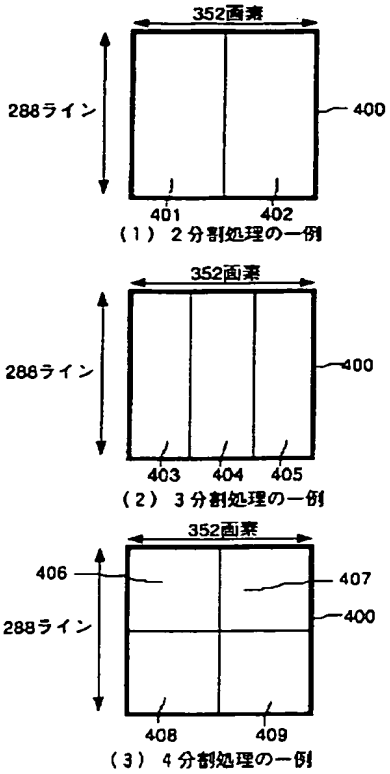
[Drawing 1]



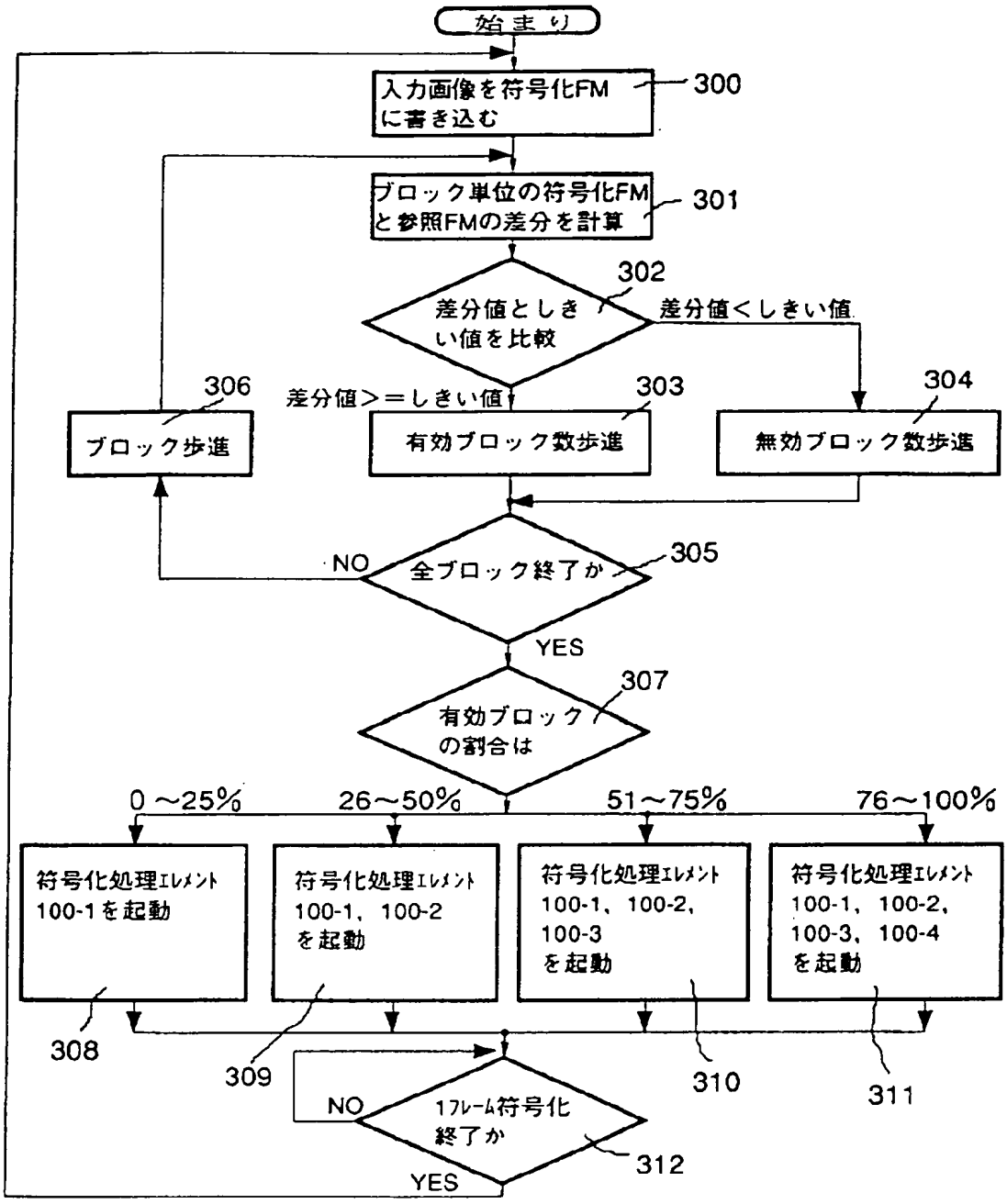
[Drawing 3]



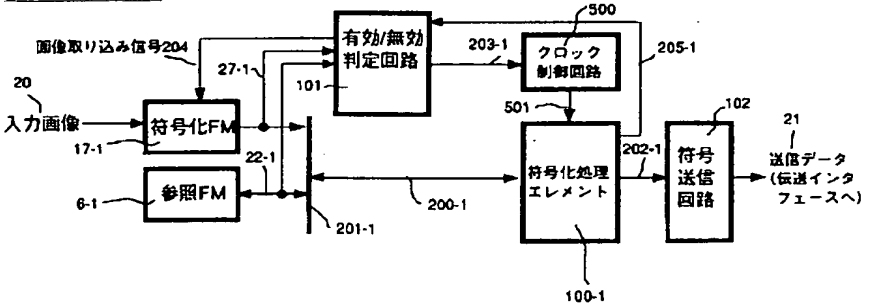
[Drawing 4]


352画素
288ライン
400
401
402
（1）２分割処理の一例
352画素
288ライン
400
403
404
405
（2）３分割処理の一例
352画素
406
407
288ライン
400
408
409
（3）４分割処理の一例

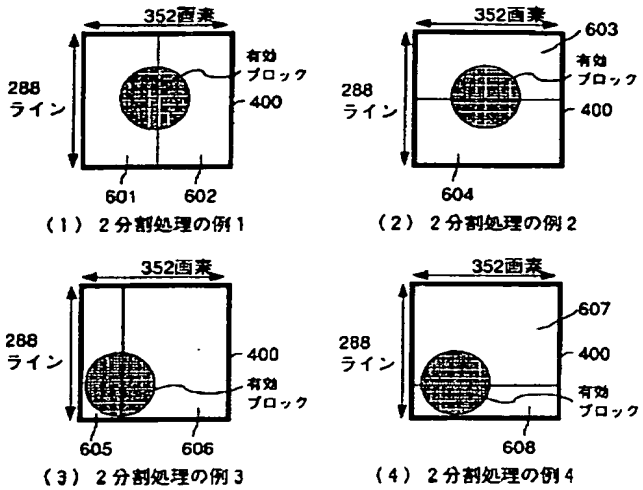
[Drawing 2]



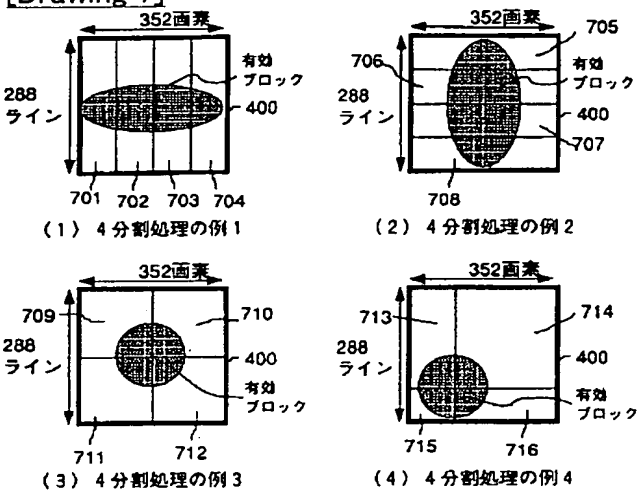
[Drawing 5]



[Drawing 6]



[Drawing 7]



[Translation done.]